General Description

The MAX14483 is a 6-channel, 3.75kV$_{RMS}$ digital galvanic isolator using Maxim's proprietary process technology. The six signal channels are individually optimized for SPI applications and include very low propagation delay on the SDI, SDO, and SCLK channels. The SDO channel's tri-state control is enabled by the $\overline{CS}$ input as well as a second enable control input pin ($\overline{SDOEN}$), allowing a single MAX14483 to isolate multiple SPI devices. To simplify system design, an open-drain $\overline{FAULT}$ output can be wire ORed with error outputs from other devices. In addition, an auxiliary channel (AUX) is available for passing timing or control signals from the master side to the slave side and power monitors (SAA, SBA) are provided for both power domains to signal if the opposite side of the isolator is ready for operation. Independent 1.71V to 5.5V supplies on each side of the isolator also make the device suitable for use as a level translator.

The MAX14483 has an isolation rating of 3.75kV$_{RMS}$ for 60 seconds and is available in a 20-pin SSOP package with 5.5mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 400V, which gives it a group 2 rating in creepage tables.

The MAX14483 is rated for operation at ambient temperatures of -40°C to +125°C.

Applications

- Programmable Logic Controllers
- Industrial Automation
- Process Automation
- Building Automation
- Robotics
- General SPI-bus Isolation

Benefits and Features

- Saves Space and Components
  - 6 Isolated Channels in a 20-SSOP Package
- Low Propagation Delay on SCLK, SDI, and SDO
  - Up to 100MHz Clock, 200Mbps Data Rate
  - 10ns Typical Propagation Delay
  - 2ns Maximum Pulse Width Distortion
  - 250ps Typical Peak Jitter
- Robust Galvanic Isolation of Digital Signals
  - Withstands 3.75kV$_{RMS}$ for 60s (V_{ISO})
  - Continuously Withstands 450V$_{RMS}$ (V_{IOWM})
  - Withstands ±10kV Surge between GNDA and GNDB with 1.2/50μs Waveform
  - High CMTI (50kV/μs, Typical)
- Flexible System Design
  - Wide 1.71V to 5.5V Voltage Range on Each Side
  - $\overline{SDOEN}$ Control Pin for Sharing Isolators
  - Open-Drain $\overline{FAULT}$ Channel for Shared Interrupt on Master Side
  - Auxiliary Channel for Timing or Control
- Low Power Consumption
  - 1.53mW per Channel at SCLK = 10MHz with V_{DD} = 3.3V
  - 0.77mW per Channel at SCLK = 10MHz with V_{DD} = 1.8V

Safety Regulatory Approvals (Pending)

- UL According to UL1577
- cUL According to CSA Bulletin 5A

***Ordering Information* and *Typical Operating Circuits* appear at end of data sheet.**

Absolute Maximum Ratings

V_{DDA} to GNDA, V_{DDB} to GNDB ....-0.3V to +6V
$\overline{ICS}$, ISCLK, ISDI, IAUX, $\overline{SDOEN}$, $\overline{OFAULT}$
to GNDB ....-0.3V to +6V
OSDO, SAA to GNDB ....-0.3V to (V_{DDB} + 0.3V)
ISDO, $\overline{IFAULT}$, $\overline{IRDY}$ to GNDA...............................-0.3V to +6V
$\overline{OCS}$, OSCLK, OSDI, OAUX, SBA
to GNDA ....-0.3V to (V_{DDA} + 0.3V)
Short-Circuit Duration
$\overline{OCS}$, OSCLK, OSDI, OAUX, SBA to V_{DDA}
or GNDA ....Continuous
OSDO, SAA to V_{DDB} or GNDB ....Continuous
Short Circuit Continuous Current ($\overline{OFAULT}$).................. 100mA
Continuous Power Dissipation
Single Layer Board T_A = +70°C 640mW
Derate above +70°C...8mW/°C
Multilayer Board T_A = +70°C......................................964mW
Derate above +70°C...12mW/°C
Operating Temperature Range........................ -40°C to +125°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range .... -60°C to +150°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics

Thermal Resistance, Single Layer Board
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....125°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..............33°C/W

Thermal Resistance, Four Layer Board
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....83°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..............33°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{DDA}	Relative to GNDA		1.71		5.5	V
	V_{DDB}	Relative to GNDB		1.71		5.5	
Undervoltage-Lockout Threshold	$V_{UVLO\_}$	$V_{DD\_}$ rising		1.5	1.6	1.66	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}				45		mV
Supply Current Side A (Note 2)	I_{DDA}	$\overline{IRDY}$ = 0V, $\overline{SDOEN}$ = 0V, all other inputs = 500kHz square wave, C_L = 0pF	V_{DDA} = 5V		1.07	1.86	mA
			V_{DDA} = 3.3V		1.04	1.81	
			V_{DDA} = 2.5V		1.03	1.79	
			V_{DDA} = 1.8V		1.00	1.59	
		10MHz square wave on ISCLK, 5MHz square wave on ISDO and ISDI, all other inputs = 0V, C_L = 0pF	V_{DDA} = 5V		1.71	2.59	
			V_{DDA} = 3.3V		1.46	2.32	
			V_{DDA} = 2.5V		1.39	2.21	
			V_{DDA} = 1.8V		1.30	1.94	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current Side B (Note 2)	I_{DDB}	$\overline{IRDY}$ = 0V, $\overline{SDOEN}$ = 0V, all other inputs = 500kHz square wave, C_L = 0pF	V_{DDB} = 5V		0.92	1.64	mA
			V_{DDB} = 3.3V		0.90	1.59	
			V_{DDB} = 2.5V		0.88	1.57	
			V_{DDB} = 1.8V		0.86	1.27	
		10MHz square wave on ISCLK, 5MHz square wave on ISDO and ISDI, all other inputs = 0V, C_L = 0pF	V_{DDB} = 5V		1.46	2.30	
			V_{DDB} = 3.3V		1.33	2.18	
			V_{DDB} = 2.5V		1.33	2.14	
			V_{DDB} = 1.8V		1.28	1.80	
LOGIC INPUTS AND OUTPUTS							
Input High Voltage	V_{IH}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		0.7 x $V_{DD\_}$			V
		1.71V ≤ $V_{DD\_}$ < 2.25V		0.75 x $V_{DD\_}$			
Input Low Voltage	V_{IL}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V				0.8	V
		1.71V ≤ $V_{DD\_}$ < 2.25V				0.7	
Input Hysteresis	V_{HYS}				410		mV
Input Pullup Current (Note 3)	I_{PU}	IAUX, $\overline{ICS}$, $\overline{SDOEN}$, $\overline{IRDY}$		-10	-5	-1.5	μA
Input Pulldown Current (Note 3)	I_{PD}	$\overline{IFAULT}$, ISDO, ISDI, ISCLK		1.5	5	10	μA
Input Capacitance	C_{IN}	f_{SW} = 1MHz			2		pF
Output Voltage High (Note 3)	V_{OH}	$V_{O\_}$ relative to GND_ $I_{O\_}$ = 4mA source		$V_{DD\_}$ - 0.4			V
Output Voltage Low (Note 3)	V_{OL}	$V_{O\_}$ relative to GND_ $I_{O\_}$ = 4mA sink				0.4	V
Output High-Impedance Leakage Current (Note 3)	I_{OL}	OSDO, $\overline{OFAULT}$		-1		1	μA

Dynamic Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOW DATA RATE CHANNELS - $\overline{IFAULT}$, $\overline{OFAULT}$, IAUX, OAUX, $\overline{ICS}$, $\overline{OCS}$						
Common-Mode Transient Immunity	CMTI	I_ = GND_ or $V_{DD\_}$ (Note 4)		50		kV/µs
Maximum Data Rate	DR_{MAX}		25			Mbps
Minimum Pulse Width	PW_{MIN}	I_ to O_			40	ns
Glitch Rejection		I_ to O_	10	17	29	ns
Propagation Delay (Figure 1)	t_{PLH}	I_ to O_, C_L = 15pF, 4.5V ≤ $V_{DD\_}$ ≤ 5.5V	17.4	23.9	32.5	ns
		I_ to O_, C_L = 15pF, 3.0V ≤ $V_{DD\_}$ ≤ 3.6V	17.6	24.4	33.7	ns
		I_ to O_, C_L = 15pF, 2.25V ≤ $V_{DD\_}$ ≤ 2.75V	18.3	25.8	36.7	ns
		I_ to O_, C_L = 15pF, 1.71V ≤ $V_{DD\_}$ ≤ 1.89V	20.7	29.6	43.5	ns
		$\overline{IFAULT}$ to $\overline{OFAULT}$, Open drain output, R_{pullup} = 10kΩ, C_L = 15pF		150		ns
	t_{PHL}	I_ to O_, C_L = 15pF, 4.5V ≤ $V_{DD\_}$ ≤ 5.5V	16.9	23.4	33.6	ns
		I_ to O_, C_L = 15pF, 3.0V ≤ $V_{DD\_}$ ≤ 3.6V	17.2	24.2	35.1	ns
		I_ to O_, C_L = 15pF, 2.25V ≤ $V_{DD\_}$ ≤ 2.75V	17.8	25.4	38.2	ns
		I_ to O_, C_L = 15pF, 1.71V ≤ $V_{DD\_}$ ≤ 1.89V	19.8	29.3	45.8	ns
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$		0.4	4	ns
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			15.1	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			15	ns
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			15.4	ns
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			20.5	ns
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			13.9	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			14.2	ns
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			16	ns
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			21.8	ns
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V			2	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V			2	ns

Dynamic Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				13.9	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				14.2	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				19.4	
	t_{SCOHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				13	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				12.9	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				14.4	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				20.1	
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	25Mbps			250		ps
Rise Time (Figure 1)	t_R	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				1.6	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				2.2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				3	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				4.5	
Fall Time (Figure 1)	t_F	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				1.4	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				2.8	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				5.1	
SPI DATA RATE CHANNELS - ISDI, OSDI, ISDO, OSDO, ISCLK, OSCLK							
Common-Mode Transient Immunity	CMTI	I_ = GND_ or $V_{DD\_}$ (Note 4)			50		kV/µs
Maximum Data Rate	DR_{MAX}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		200			Mbps
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V		150			
Minimum Pulse Width	PW_{MIN}	I_ to O_	2.25V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			6.67	
Propagation Delay (Figure 1)	t_{PLH}	I_ to O_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.1	5.4	9.2	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	4.2	5.9	10.2	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	4.9	7.1	13.4	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.1	10.9	20.3	
	t_{PHL}	I_ to O_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.3	5.6	9.4	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	4.4	6.2	10.5	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	5.1	7.3	14.1	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.2	10.9	21.7	
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$			0.3	2	ns

Dynamic Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				3.7	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.3	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				6	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				10.3	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				3.8	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				6.5	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				11.5	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}					2	ns
	t_{SCSHL}					2	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				2.9	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				3.4	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				4.9	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				10.2	
	t_{SCOHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				3.2	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				3.8	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				5.3	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				10.9	
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	200Mbps			250		ps
Clock Jitter RMS	$T_{JCK(RMS)}$	500kHz Clock Input, Rising/Falling Edges			6.5		ps
Rise Time	t_R	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				1.6	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				2.2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				3	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				4.5	
Fall Time	t_F	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				1.4	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				2.8	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				5.1	
Enable to Data Valid	t_{EN}	$\overline{ICS}$ or $\overline{SDOEN}$ falling to OSDO valid, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			31.3	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			34.8	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			40.0	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			51.8	
Disable to Tri-state	t_{TRI}	$\overline{ICS}$ or $\overline{SDOEN}$ rising to OSDO tristate, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			33.9	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			38.6	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			44.4	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			55	

Dynamic Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL AND MONITOR CHANNELS - $\overline{\text{IRDY}}$, $\overline{\text{SDOEN}}$, SAA, SBA						
Common-Mode Transient Immunity	CMTI	I_ = GND_ or $V_{DD\_}$ (Note 4)		50		kV/µs
Glitch Rejection		$\overline{\text{SDOEN}}$	10	17	29	ns
Propagation Delay	t_{PLH}	$\overline{\text{IRDY}}$ low to high		100		µs
	t_{PHL}	$\overline{\text{IRDY}}$ high to low		100		
Rise Time	t_R	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.6	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			2.2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			3	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			4.5	
Fall Time	t_F	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.4	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			2	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			2.8	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			5.1	

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Not production tested. Guaranteed by design and characterization.
Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.
Note 4: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

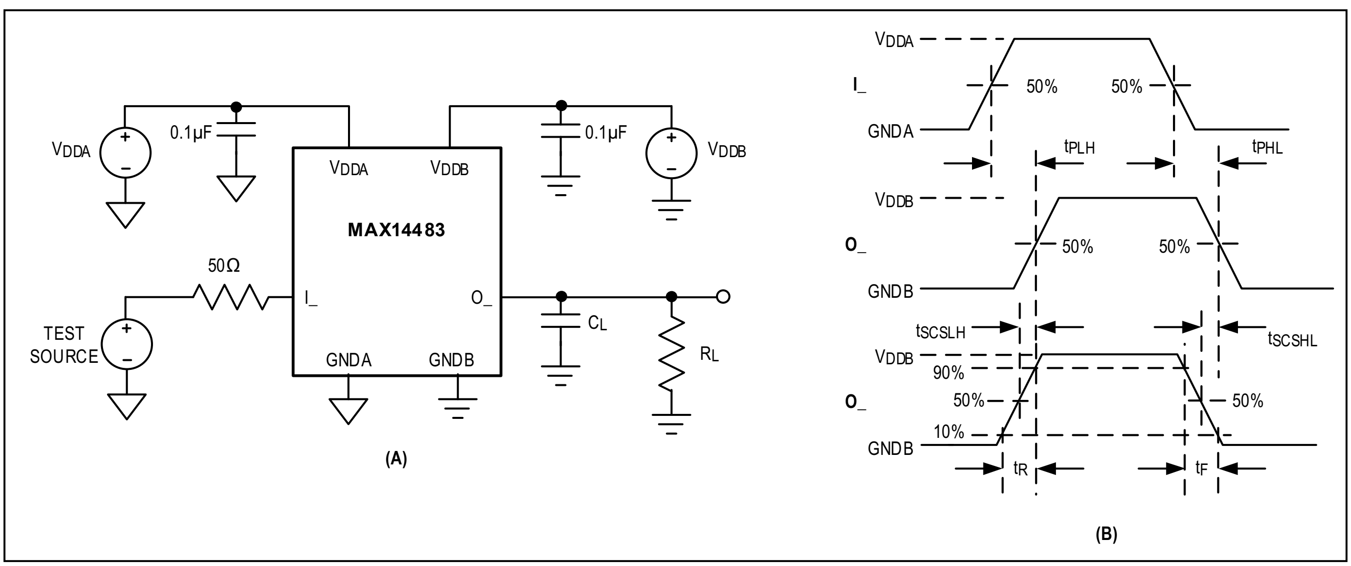


Figure 1. Test Circuit (A) and Timing Diagram (B)

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, all pins		±4		kV

Insulation Characteristics

Table 1. 20-pin SSOP Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1050	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 5)	560	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 5)	400	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	5300	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 5, 6)	3750	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic Insulation, 1.2/50µs pulse per IEC61000-4-5	10	kV
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500V, T_S = 150°C	$>10^{9}$	
Barrier Capacitance Side A to Side B	CIO	f_{SW} = 1MHz (Note 7)	1.5	pF
Minimum Creepage Distance	CPG	SSOP	5.5	mm
Minimum Clearance Distance	CLR	SSOP	5.5	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	>400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 5: V_{ISO}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.
Note 6: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 7: Capacitance is measured with all pins on side A and side B tied together.

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX14483 could dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. Table 2 shows the safety limits for the MAX14483.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Thermal Characteristics* section of the datasheet and power dissipation calculations are discussed in the Calculating Power Dissipation section. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 2 and Figure 3 show the thermal derating curve for safety limiting the power and the current of the device. Ensure that the junction temperature does not exceed 150°C.

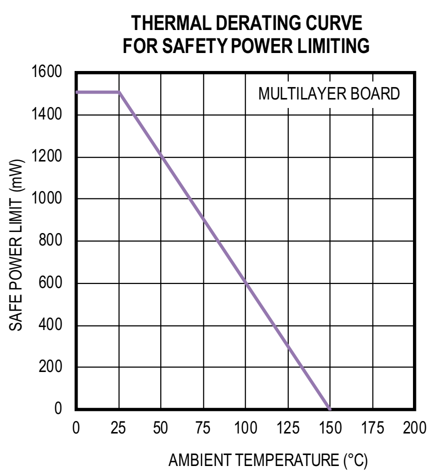


Figure 2. Thermal Derating Curve for Safety Power Limiting

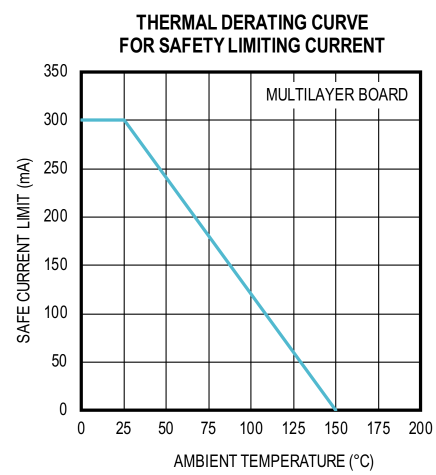


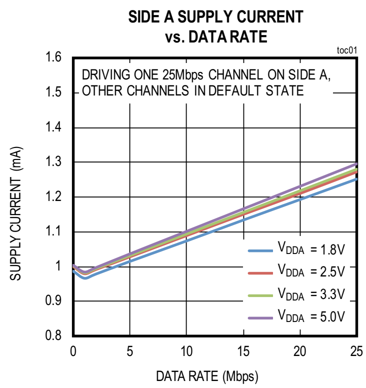
Figure 3. Thermal Derating Curve for Safety Current Limiting

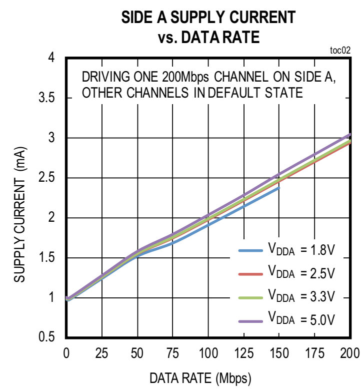
Table 2. Safety Limiting Values for the MAX14483

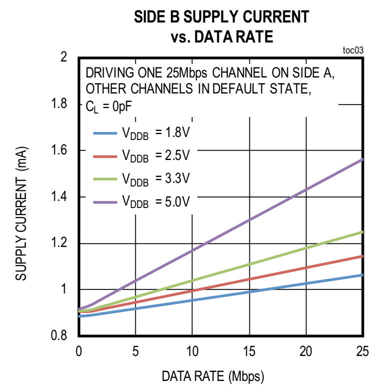
PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Safety Current on Any Pin	I_S	T_J = 150°C, T_A = 25°C, Multilayer Board	300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C, Multilayer Board	1506	mW
Maximum Safety Temperature	T_S		150	°C

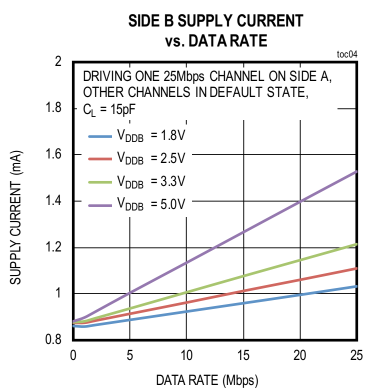
Typical Operating Characteristics

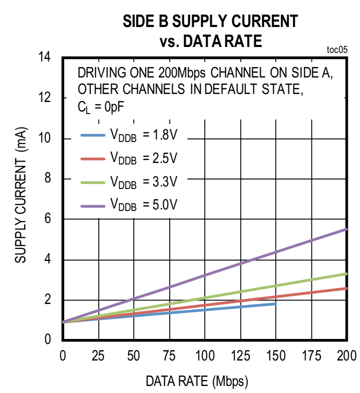
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

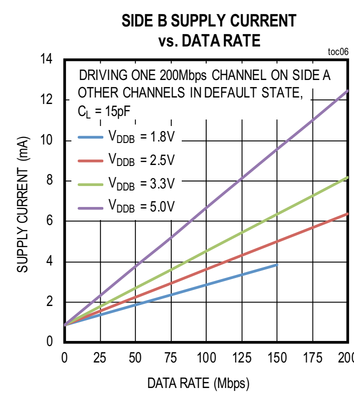


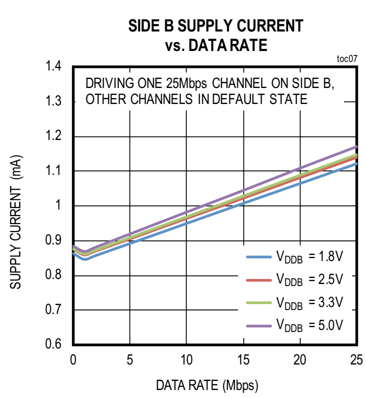


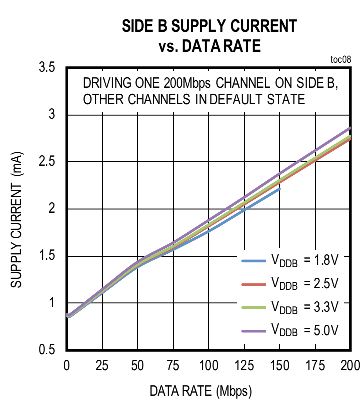


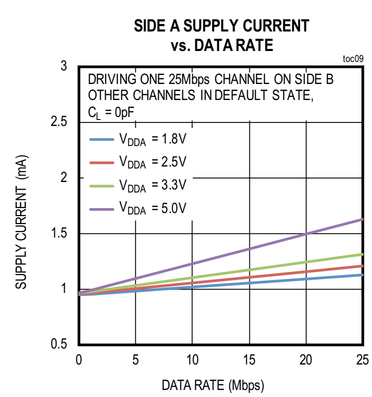






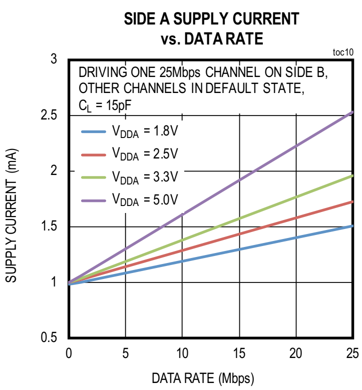


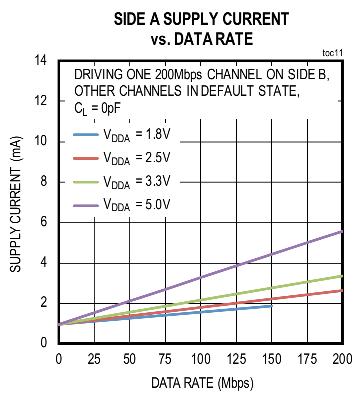


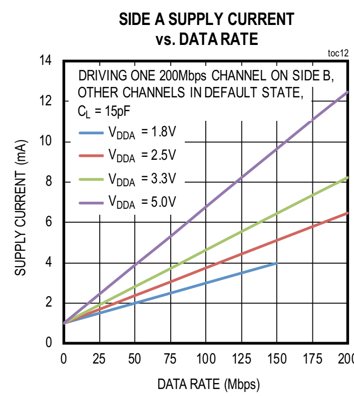


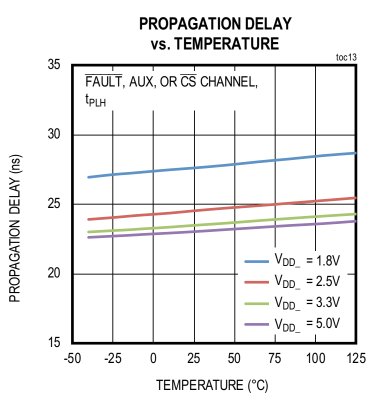
Typical Operating Characteristics (continued)

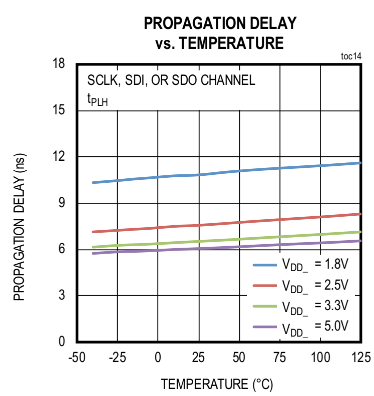
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

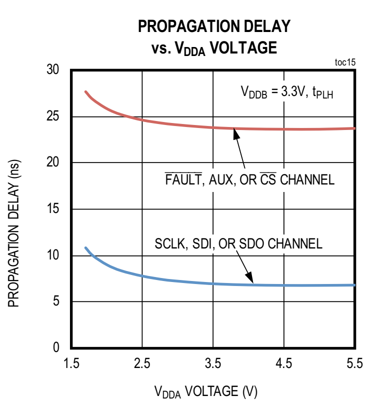


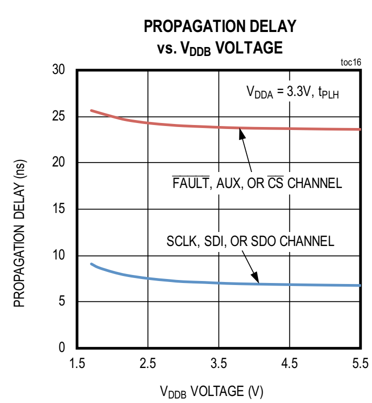








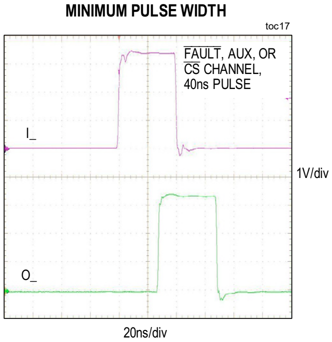




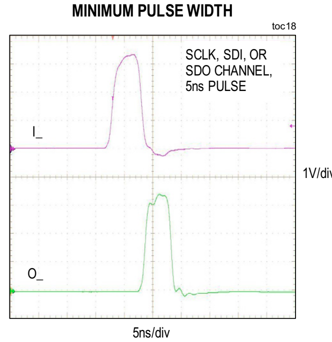
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

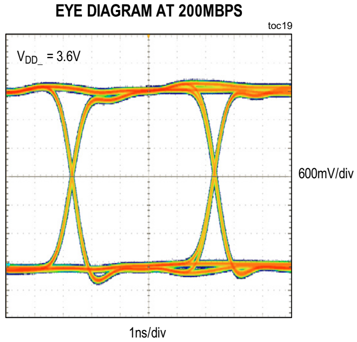
MINIMUM PULSE WIDTH



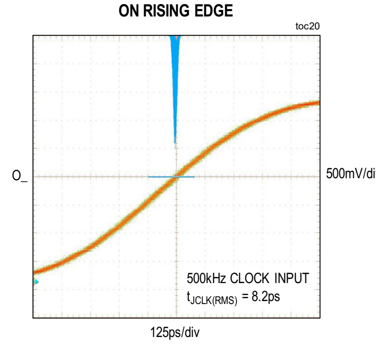
MINIMUM PULSE WIDTH



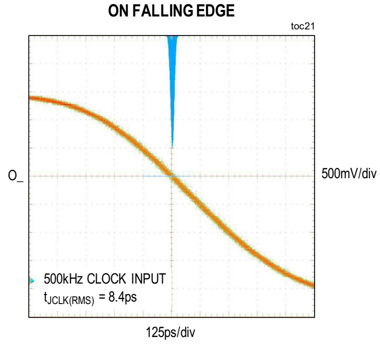
EYE DIAGRAM AT 200MBPS



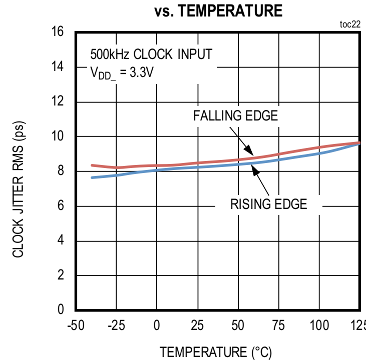
CLOCK JITTER RMS ON RISING EDGE



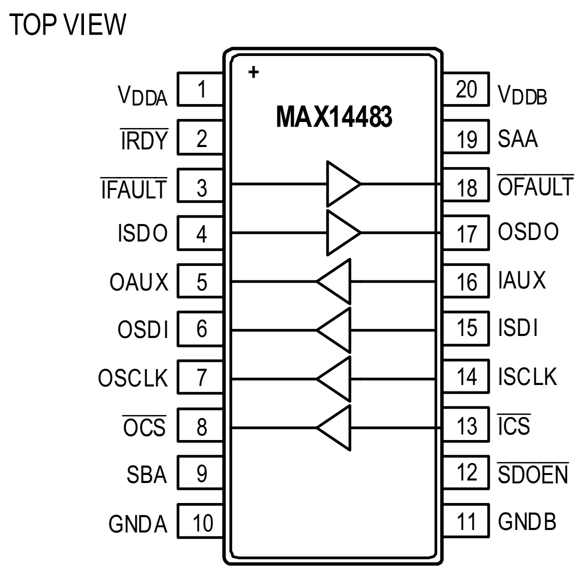
CLOCK JITTER RMS ON FALLING EDGE



CLOCK JITTER RMS vs. TEMPERATURE



Pin Configurations



20 SSOP

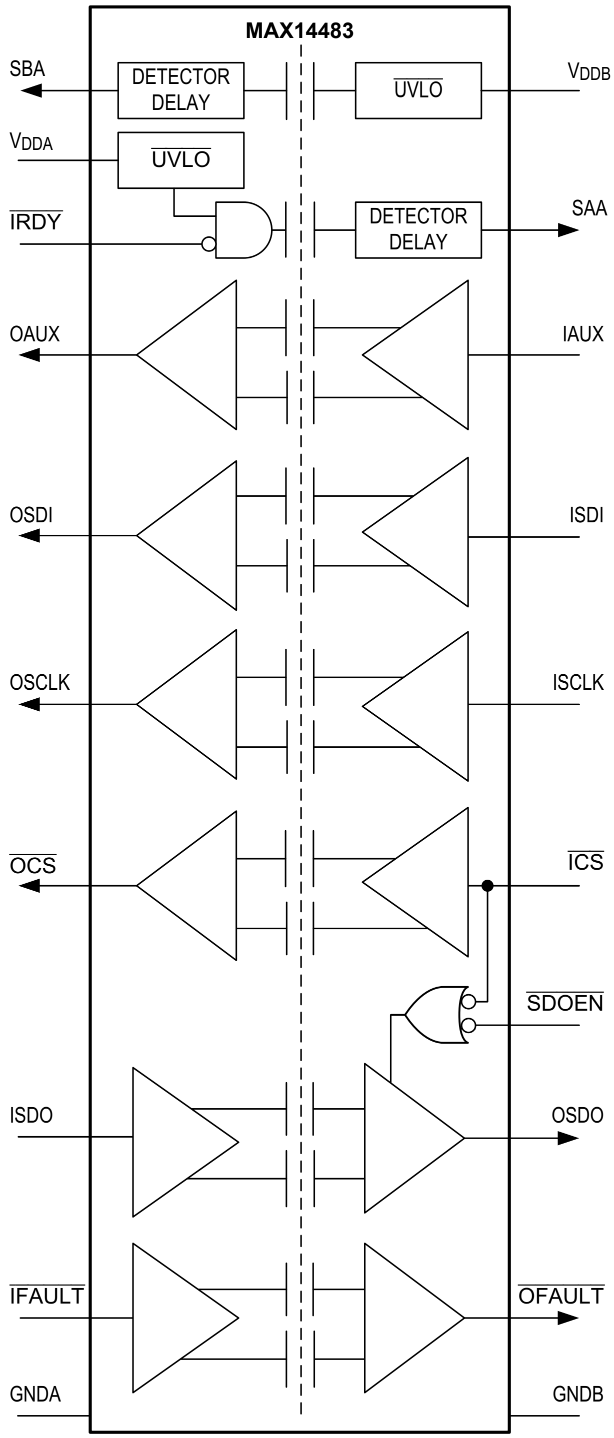
Pin Description

PIN	NAME	FUNCTION	REFERENCE
SIDE A (SPI SLAVE)			
1	V_{DDA}	Power Supply. Bypass V_{DDA} with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDA
2	$\overline{\text{IRDY}}$	Ready Input. Assert $\overline{\text{IRDY}}$ low when Side A is ready for communication. When $\overline{\text{IRDY}}$ is high, SAA is low and Side B outputs are in their default state ($\overline{\text{OFAULT}}$ is low and OSDO is low when enabled). When $\overline{\text{IRDY}}$ is low, and Side A power is valid, SAA is high and Side B outputs operate normally. If the ready function is not required, tie $\overline{\text{IRDY}}$ to GNDA.	GNDA
3	$\overline{\text{IFAULT}}$	Input to $\overline{\text{FAULT}}$ channel; has a weak internal pulldown.	GNDA
4	ISDO	Input to SDO channel; has a weak internal pulldown. Connect to MISO of slave device(s).	GNDA
5	OAUX	Output of AUX channel.	GNDA
6	OSDI	Output of SDI channel. Connect to MOSI of slave device(s).	GNDA
7	OSCLK	Output of SCLK channel. Connect to SCLK of slave device(s).	GNDA
8	$\overline{\text{OCS}}$	Output of $\overline{\text{CS}}$ channel. Connect to $\overline{\text{CS}}$ of slave device(s).	GNDA

Pin Description (continued)

PIN	NAME	FUNCTION	REFERENCE
9	SBA	Side B Active. SBA is high when Side B has power and is operating normally. When Side B is not powered, SBA is set low and all Side A outputs are in their default state. A nominal 100µs delay is added between the detection of Side B power and the assertion of SBA. This allows time for the power supply to settle, and ensures a minimum low pulse width for SBA.	GNDA
10	GNDA	Power and Signal Ground for Side A	GNDA
SIDE B (SPI MASTER)			
20	V_{DDB}	Power Supply. Bypass V_{DDB} with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDB
19	SAA	Side A Active. SAA is high when Side A has power, is operating normally, and $\overline{\text{IRDY}}$ is low. When Side A is not powered, SAA is set low and all Side B outputs are in their default state ($\overline{\text{OFAULT}}$ is low and OSDO is low when enabled). A nominal 100µs delay is added between the detection of Side A power and the assertion of SAA. This allows time for the power supply to settle, and ensures a minimum low pulse width for SAA.	GNDB
18	$\overline{\text{OFAULT}}$	Output of $\overline{\text{FAULT}}$ channel. Open Drain Output	GNDB
17	OSDO	Output of SDO channel. Tri-stated when $\overline{\text{ICS}}$ and $\overline{\text{SDOEN}}$ are both high. Connect to MISO of SPI master.	GNDB
16	IAUX	Input to AUX channel; has a weak internal pullup to V_{DDB}	GNDB
15	ISDI	Input to SDI channel; has a weak internal pulldown. Connect to MOSI of SPI master.	GNDB
14	ISCLK	Input to SCLK channel; has a weak internal pulldown. Connect to SCLK of SPI master.	GNDB
13	$\overline{\text{ICS}}$	Input to $\overline{\text{CS}}$ channel; has a weak internal pullup to V_{DDB}. Connect to $\overline{\text{CS}}$ output or GPO of SPI master. When $\overline{\text{ICS}}$ is low, OSDO output is enabled.	GNDB
12	$\overline{\text{SDOEN}}$	SDO Enable; has a weak internal pullup to V_{DDB}. When $\overline{\text{SDOEN}}$ is low, the OSDO output is enabled, allowing the SDO channel to be used with multiple side A SPI slaves.	GNDB
11	GNDB	Power and Signal Ground for Side B	GNDB

Functional Diagram



Detailed Description

The MAX14483 is a 6-channel, 3.75kV$_{RMS}$ digital galvanic isolator using Maxim's proprietary process technology. The six signal channels are individually optimized for SPI applications and include very low propagation delay on the SDI, SDO, and SCLK channels. The SDO channel's tri-state control is enabled by the $\overline{CS}$ input as well as a second enable control input pin ($\overline{SDOEN}$), allowing a single MAX14483 to isolate multiple SPI devices. To simplify system design, an open drain $\overline{FAULT}$ output can be wire ORed with error outputs from other devices. In addition, an auxiliary channel (AUX) is available for passing timing or control signals from the master side to the slave side and power monitors (SAA, SBA) are provided for both power domains to signal that the opposite side of the isolator is ready for operation. Independent 1.71V to 5.5V supplies on each side of the isolator also make the device suitable for use as a level translator.

The MAX14483 offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The device isolates different ground domains and blocks high-voltage/high-current transients from sensitive or human interface circuitry.

The MAX14483 is available with a maximum data rate of 200Mbps (SPI Data Rate Channels). The device has two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively.

The MAX14483 also features an internal refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The MAX14483 provides galvanic isolation for digital signals that are transmitted between two ground domains. The device withstands up to 560V$_{PEAK}$ of continuous isolation and up to 3.75kV$_{RMS}$ for up to 60 seconds in the 20-pin SSOP package, which has 5.5mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 400V, giving it a group 2 rating in creepage tables.

Level-Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX14483 to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Isolation Channels

The MAX14483 has three types of channels (Table 3). Low Data Rate Channels are $\overline{FAULT}$, AUX and $\overline{CS}$. SPI Data Rate Channels are SCLK, SDI, and SDO. Control and Monitor Channels are $\overline{IRDY}$, $\overline{SDOEN}$, SAA and SBA. Different types of channels have different electrical specifications.

Low Data Rate Channels

The Low Data Rate Channels are $\overline{FAULT}$, AUX, and $\overline{CS}$. Each channel is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each channel has a maximum data rate of 25Mbps. The $\overline{FAULT}$ and AUX channels are designed to support SPI devices which require control signals beyond the standard 4-wire SPI bus. The output drivers of AUX and $\overline{CS}$ channels are push-pull, eliminating the need for pullup resistors. The $\overline{FAULT}$ channel output is open drain and requires a pullup resistor. All the outputs are able to drive both TTL and CMOS logic inputs. The input channels have an integrated glitch filter to help operate in noisy environments and avoid false triggering.

SPI Data Rate Channels

The SPI Data Rate Channels are SCLK, SDI, and SDO; these channels are designed to support standard 4-wire SPI bus signals ($\overline{CS}$ is considered as a Low Data Rate Channel). Each channel is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each channel has been optimized for fast data rate and minimal skew between channels, with a maximum data rate of 200Mbps and maximum channel-to-channel propagation delay skew of only 10.2ns with $V_{DD\_}$ = 1.8V. The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Control and Monitor Channels

The Control and Monitor Channels are $\overline{\text{IRDY}}$, $\overline{\text{SDOEN}}$, SAA and SBA. Each channel is unidirectional; it only passes data in one direction, as indicated in the functional diagram. The monitor channels (SAA, SBA) are designed to pass essentially DC signals and have significantly longer propagation delays than other channels, meaning they should not be used for data signals. The outputs are able to drive both TTL and CMOS logic inputs. SAA and SBA are set high when their respective opposite side of the isolator has power and is operating normally. When Side A or Side B is not powered, SAA or SBA is set low and all outputs are set to their default state (OSDO is high impedance when disabled). A nominal 100µs delay is added between the detection of the opposite side power and the assertion of SAA or SBA. This allows time for the power supply to settle, and ensures a minimum low pulse width for SAA and SBA.

The control channels ($\overline{\text{IRDY}}$, $\overline{\text{SDOEN}}$) have an integrated glitch filter. $\overline{\text{IRDY}}$ is an external input from the A side circuits (such as a Digital I/O device) to indicate that these devices are powered and active, allowing the B side circuit (such as a MCU SPI Master) to initiate data transfer across the isolation barrier. $\overline{\text{SDOEN}}$ is an output enable control for OSDO. $\overline{\text{SDOEN}}$ allows the B side of the MAX14483 to be shared with multiple SPI devices on the A side by enabling OSDO when $\overline{\text{ICS}}$ is not asserted. The A side SPI devices can be configured either in the daisy chain mode, where a single $\overline{\text{CS}}$ signal enables all Side A devices as well as the OSDO output, or in the independent slave mode, where one Side A device uses the $\overline{\text{CS}}$ channel in the MAX14483 and the rest of the Side A devices have their own $\overline{\text{CS}}$ isolator channels, external to the MAX14483. The independent slave mode requires OSDO to be enabled any time one of the $\overline{\text{CS}}$ signals is asserted, which can be accomplished by

Table 3. Channel Summary

CHANNEL TYPE	CHANNEL	OUTPUT DEFAULT	INPUT CURRENT SOURCE	GLITCH FILTER
Low Data Rate	$\overline{\text{FAULT}}$	Low	Pull Down	Yes
Low Data Rate	AUX	High	Pull Up	Yes
Low Data Rate	$\overline{\text{CS}}$	High	Pull Up	Yes
SPI Data Rate	SDI	Low	Pull Down	No
SPI Data Rate	SCLK	Low	Pull Down	No
SPI Data Rate	SDO	Low	Pull Down	No
Control and Monitor	$\overline{\text{SDOEN}}$	Input Only	Pull Up	Yes
Control and Monitor	$\overline{\text{IRDY}}$	Input Only	Pull Up	Yes
Control and Monitor	SAA	High when Side A has power, is operating normally, and $\overline{\text{IRDY}}$ is low. Low when Side A is not powered or $\overline{\text{IRDY}}$ is high.	N/A	N/A
Control and Monitor	SBA	High when Side B has power and is operating normally. Low when Side B is not powered.	N/A	N/A

Table 4. Output Behavior During Undervoltage Conditions

$V_{IN\_}$	V_{DDA}	V_{DDB}	V_{OUTA}	SDO ENABLE	V_{OUTB}	
I_			O_		OSDO	$\overline{\text{OFAULT}}$
1	Powered	Powered	1	0	Hi-Z	1
			1	1	1	1
0	Powered	Powered	0	0	Hi-Z	0
			0	1	0	0
X	Undervoltage	Powered	Default	0	Hi-Z	Default
			Default	1	Default	Default
X	Powered	Undervoltage	Default	0	Hi-Z	Default
			Default	1	Default	Default

connecting a GPO pin to $\overline{SDOEN}$ and asserting it any time any $\overline{CS}$ signal is asserted. In the case that the B side of the MAX14483 is not shared with multiple SPI devices, there is no need for OSDO to be high impedance, and $\overline{SDOEN}$ can be permanently connected to GNDB. Refer to ***Typical Operating Circuits*** for details.

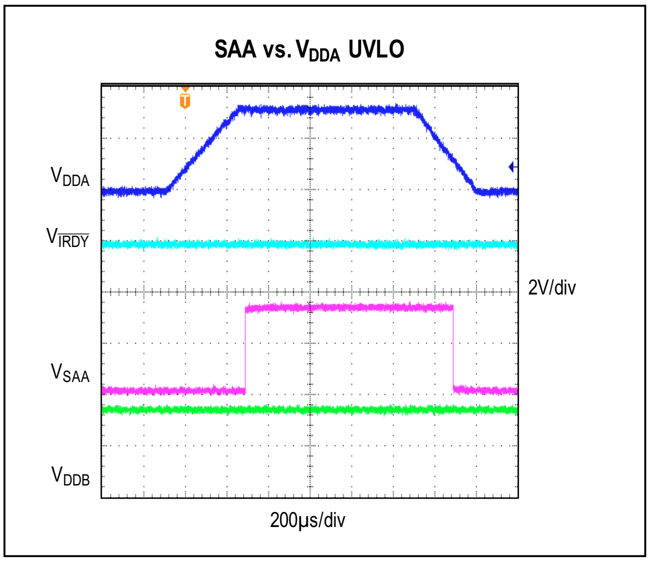


Figure 4. V_{DDA} - UVLO Controlling SAA Signal

Startup and Undervoltage-Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs (Table 4). Figure 4 through Figure 6 show the behavior of the SAA and SBA signals during power-up, power-down and $\overline{IRDY}$ toggling.

Applications Information

Power-Supply Sequencing

The MAX14483 does not require special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

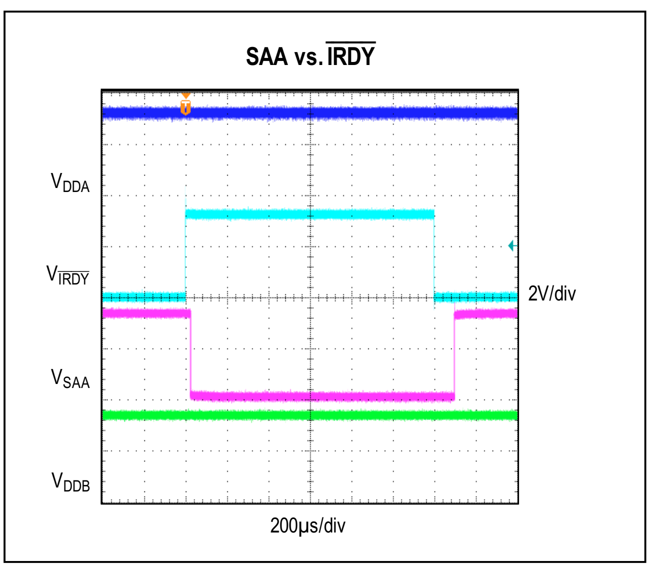


Figure 5. $\overline{IRDY}$ Controlling SAA Signal

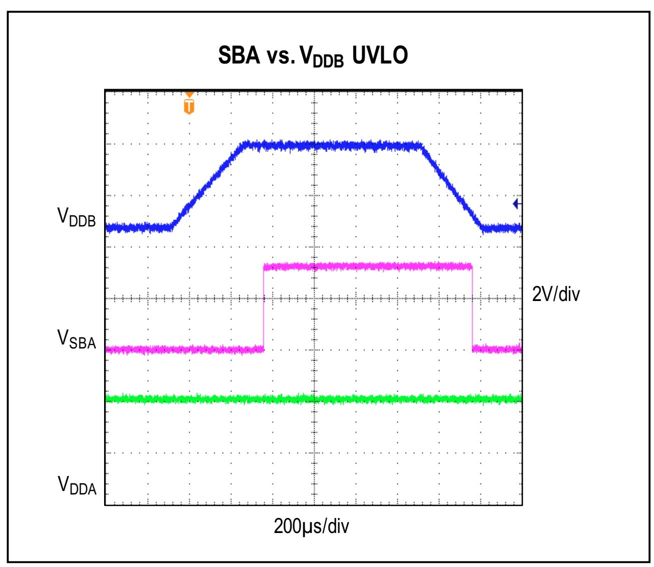


Figure 6. V_{DDB} - UVLO Controlling SBA Signal

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias to make low-inductance paths for the signals.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX14483 free from ground and signal planes. Any galvanic or metallic connection between the Side A and the Side B defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in Figure 7 and Figure 8. Please note the data in Figure 7 and Figure 8 are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the "no load" current (shown in Figure 7 and Figure 8), which is a function of Voltage and Data Rate, and the "load current", which depends on the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second / 2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD} \div R_L$$

where

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

In the case of an SPI bus which often has intermittent read or write cycles, one other factor to consider is the active duty cycle percentage as well as the typical active current.

Example (shown in Figure 9): An SPI Master running at 10MHz and with 8-bit data package. The MAX14483 is operating with V_{DDB} = 2.5V, V_{DDA}= 3.3V, SCLK operating at 20Mbps with a 15pF load, SDI and SDO channels operating in 8-bit data frame at 10Mbps with a 15pF load on each, $\overline{CS}$ operating at effective rate of 2.5Mbps (20Mbps divide by 8) with a 15pF load, and AUX channel operating at 1Mbps with a 10pF load. Channels SAA and SBA are not in use and $\overline{FAULT}$ drives a resistive load when active. Refer to Table 5 and Table 6 for V_{DDA} and V_{DDB} supply current calculation worksheets.

V_{DDA} must supply:

- ISDO operating at 3.3V and 10Mbps, consuming 0.24mA, estimated from Figure 7.
- $\overline{IFAULT}$ operating at 3.3V and DC, consuming 0.14mA, estimated from Figure 7.
- OAUX operating at 3.3V and 1Mbps, consuming 0.19mA, estimated from Figure 8. I_{CL} on OAUX for 10pF capacitor at 3.3V is 0.017mA.
- OSDI operating at 3.3V and 10Mbps, consuming 0.30mA, estimated from Figure 8. I_{CL} on OSDI for 15pF capacitor at 3.3V is 0.25mA.
- OSCLK operating at 3.3V and 20Mbps, consuming 0.42mA, estimated from Figure 8. I_{CL} on OSCLK for 15pF capacitor at 3.3V is 0.50mA.
- $\overline{OCS}$ operating at 3.3V and 2.5Mbps, consuming 0.21mA, estimated from Figure 8. I_{CL} on $\overline{OCS}$ for 15pF capacitor at 3.3V is 0.062mA.

Total current for side A = 2.33mA, typical.

V_{DDB} must supply:

- IAUX operating at 2.5V and 1Mbps, consuming 0.15mA, estimated from Figure 7.
- ISDI operating at 2.5V and 10Mbps, consuming 0.23mA, estimated from Figure 7.
- ISCLK operating at 2.5V and 20Mbps, consuming 0.33mA, estimated from Figure 7.
- $\overline{ICS}$ operating at 2.5V and 2.5Mbps, consuming 0.16mA, estimated from Figure 7.
- OSDO operating at 2.5V and 10Mbps, consuming 0.27mA, estimated from Figure 8. I_{CL} on OSDO for 15pF capacitor at 2.5V is 0.19mA.
- $\overline{OFAULT}$ operating at 2.5V and 1Mbps, consuming 0.18mA, estimated from Figure 8. I_{RL} on $\overline{OFAULT}$ for 10kΩ resistor at 2.5V is 0.25mA.

Total current for side B = 1.76mA, typical.

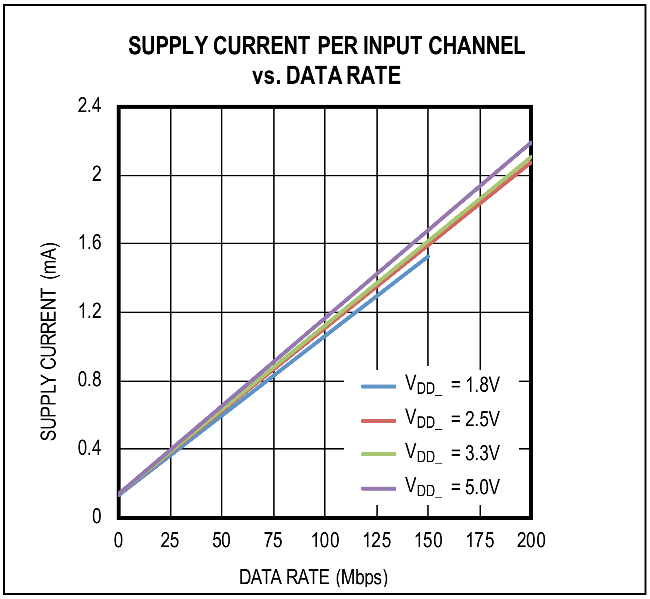


Figure 7. Supply Current Per Input Channel

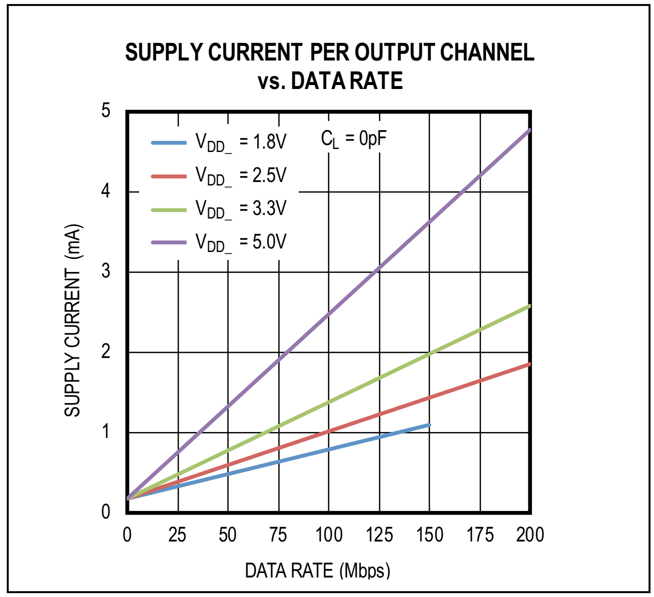


Figure 8. Supply Current Per Output Channel

Table 5. Side A Supply Current Calculation Worksheet

SIDE A	V_{DDA} = 3.3V					
Channel	**IN/OUT**	**Data Rate (Mbps)**	**Load Type**	**Load**	**“No Load” Current (mA)**	**Load Current (mA)**
OAUX	OUT	1	Capacitive	10pF	0.19	3.3V × 0.5MHz × 10pF = 0.017
OSDI	OUT	10	Capacitive	15pF	0.30	3.3V × 5MHz × 15pF = 0.25
OSCLK	OUT	20	Capacitive	15pF	0.42	3.3V × 10MHz × 15pF = 0.50
$\overline{\text{OCS}}$	OUT	2.5	Capacitive	15pF	0.21	3.3V × 1.25MHz × 15pF = 0.062
ISDO	IN	10			0.24	
$\overline{\text{IFAULT}}$	IN	0			0.14	
Total: 2.33mA						

Table 6. Side B Supply Current Calculation Worksheet

SIDE B	V_{DDB} = 2.5V					
Channel	**IN/OUT**	**Data Rate (Mbps)**	**Load Type**	**Load**	**“No Load” Current (mA)**	**Load Current (mA)**
IAUX	IN	1			0.15	
ISDI	IN	10			0.23	
ISCLK	IN	20			0.33	
$\overline{\text{ICS}}$	IN	2.5			0.16	
OSDO	OUT	10	Capacitive	15pF	0.27	2.5V × 5MHz × 15pF = 0.19
$\overline{\text{OFAULT}}$	OUT	0	Resistive	10kΩ	0.18	2.5V ÷ 10kΩ = 0.25
Total: 1.76mA						

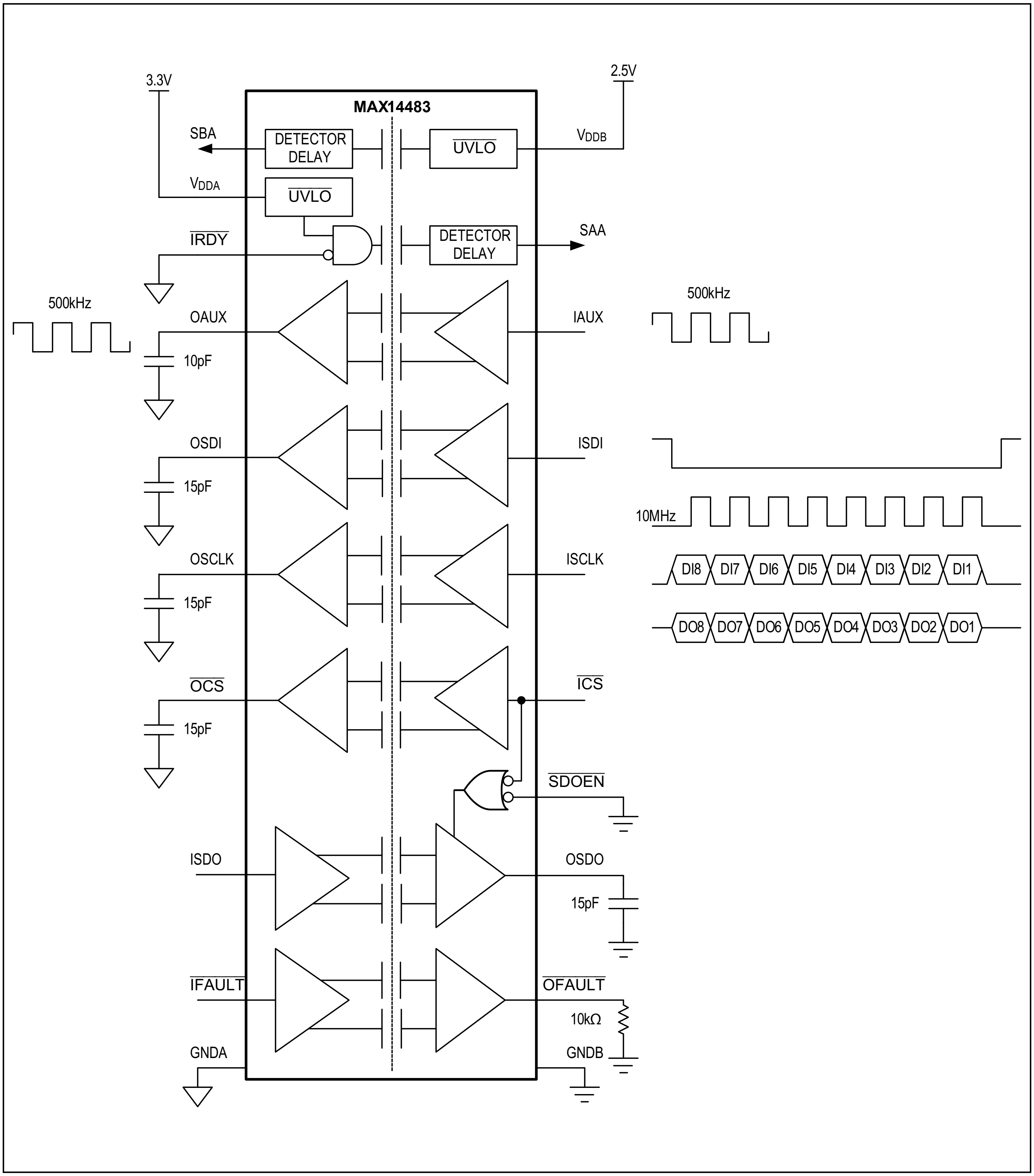
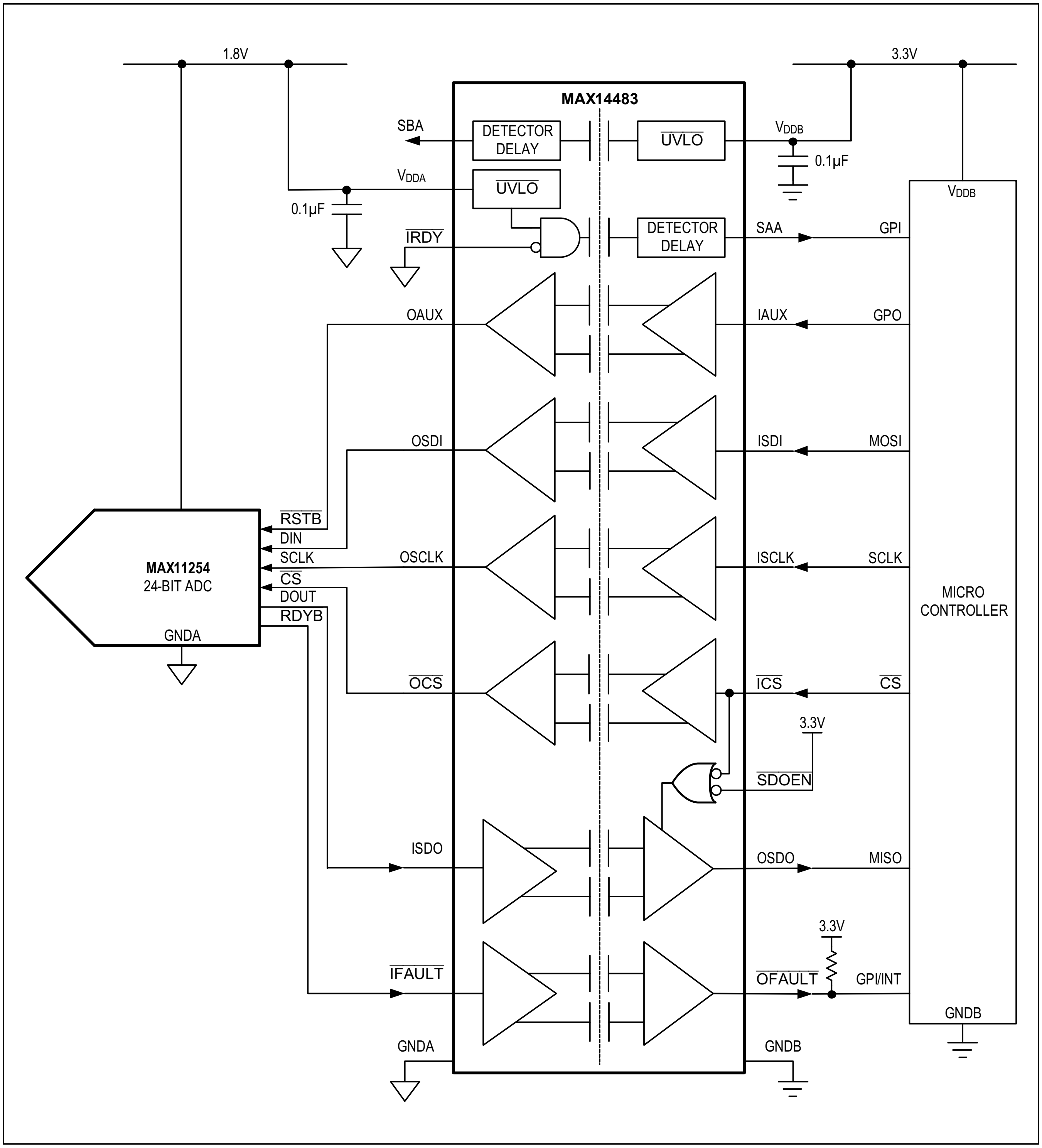


Figure 9. Example Circuit for Supply Current Calculation

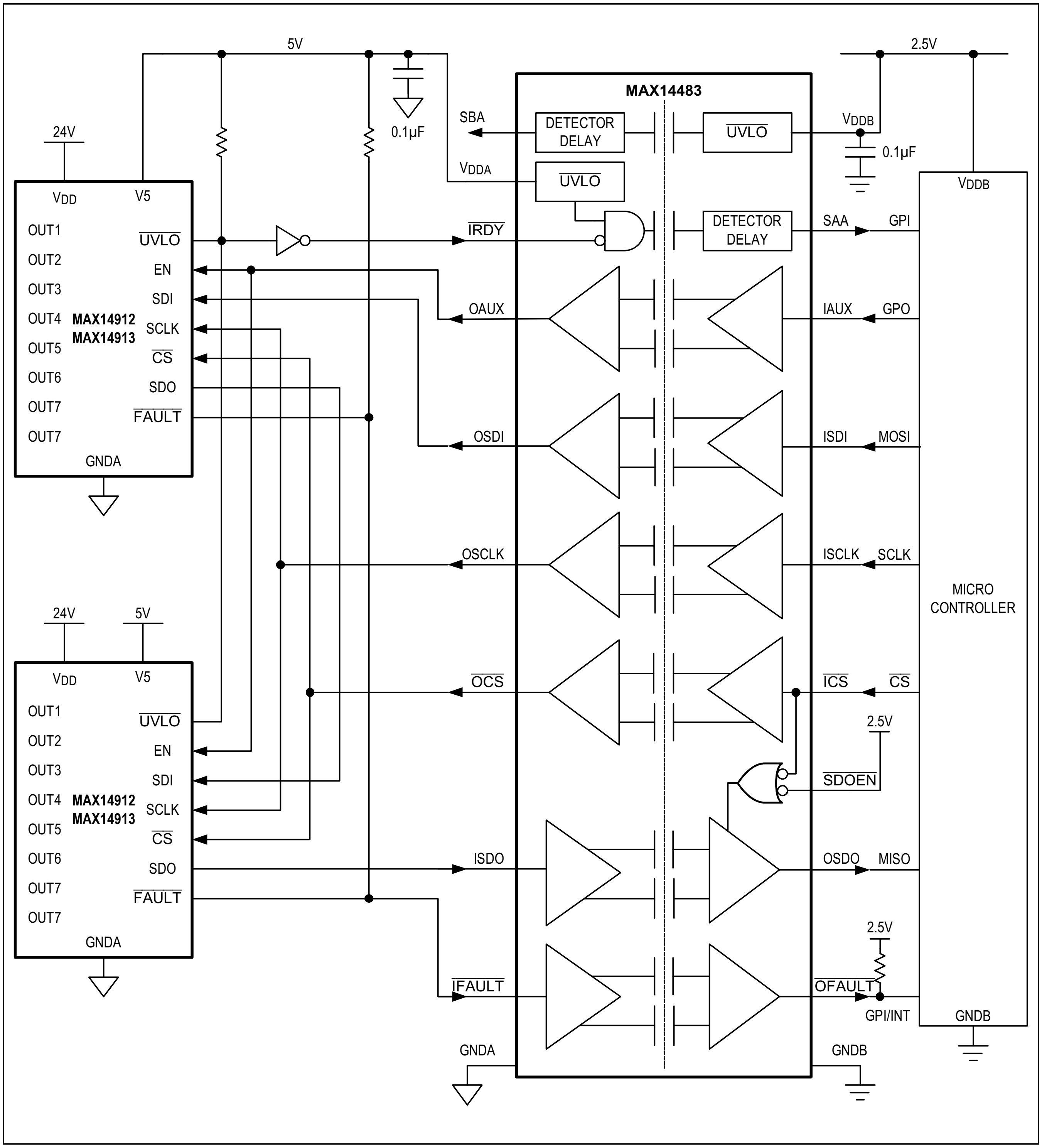
Typical Operating Circuit

Isolated SPI Interface



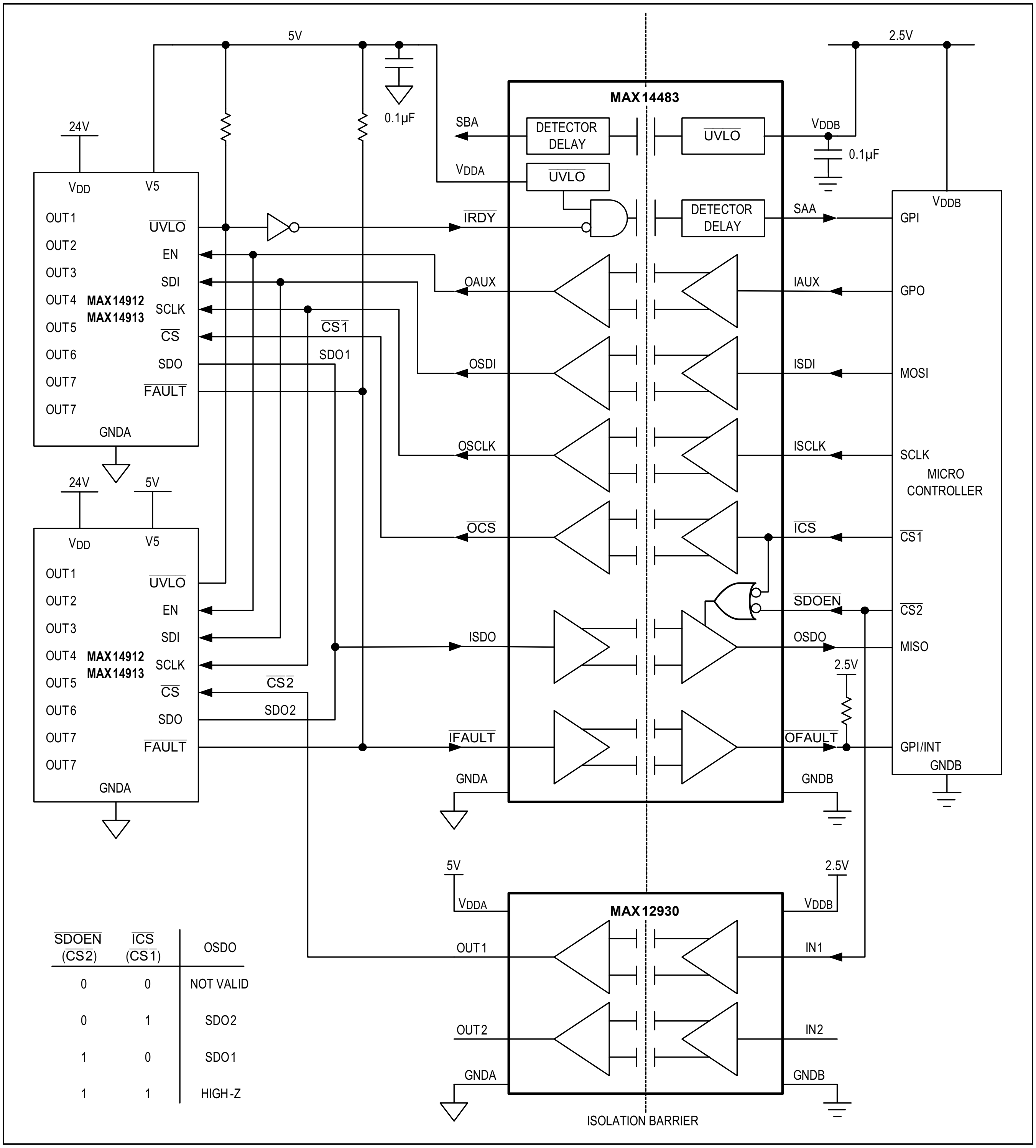
Typical Operating Circuit (continued)

Isolated SPI Daisy Chain, 16 Digital Outputs



Typical Operating Circuit (continued)

Isolated Independent Slave SPI Bus, 16 Digital Outputs



SDOEN (CS2)	ICS (CS1)	OSDO
0	0	NOT VALID
0	1	SDO2
1	0	SDO1
1	1	HIGH-Z

Ordering Information

PART	ISOLATION VOLTAGE (KVRMS)	TEMP RANGE (°C)	PIN-PACKAGE
MAX14483AAP+	3.75	-40 to +125	20-SSOP

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 SSOP	A20MS+7	21-0056	90-0094

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	08/17	Initial release	—
1	2/18	Updated *Electrical Characteristics* table, *Typical Operating Characteristics*, and *Detailed Description* section	1–20

