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Kind regards,

Team Nexperia



# PMDXB1200UPE

30 V, dual P-channel Trench MOSFET

25 March 2015

Product data sheet

## 1. General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Leadless ultra small and ultra thin SMD plastic package 1.1 x 1.0 x 0.37 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

## 3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-30	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-410	mA
<b>Static characteristics (per transistor)</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -410\text{ mA}; T_j = 25\text{ °C}$	-	1.2	1.4	$\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

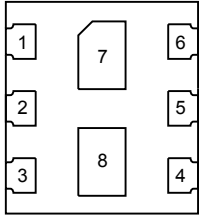
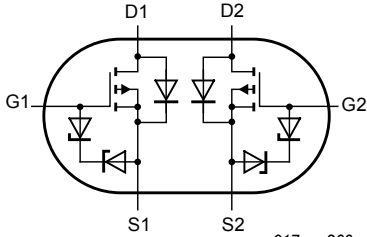


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### 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view <b>DFN1010B-6 (SOT1216)</b></p>	 <p>017aaa260</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

### 6. Ordering information

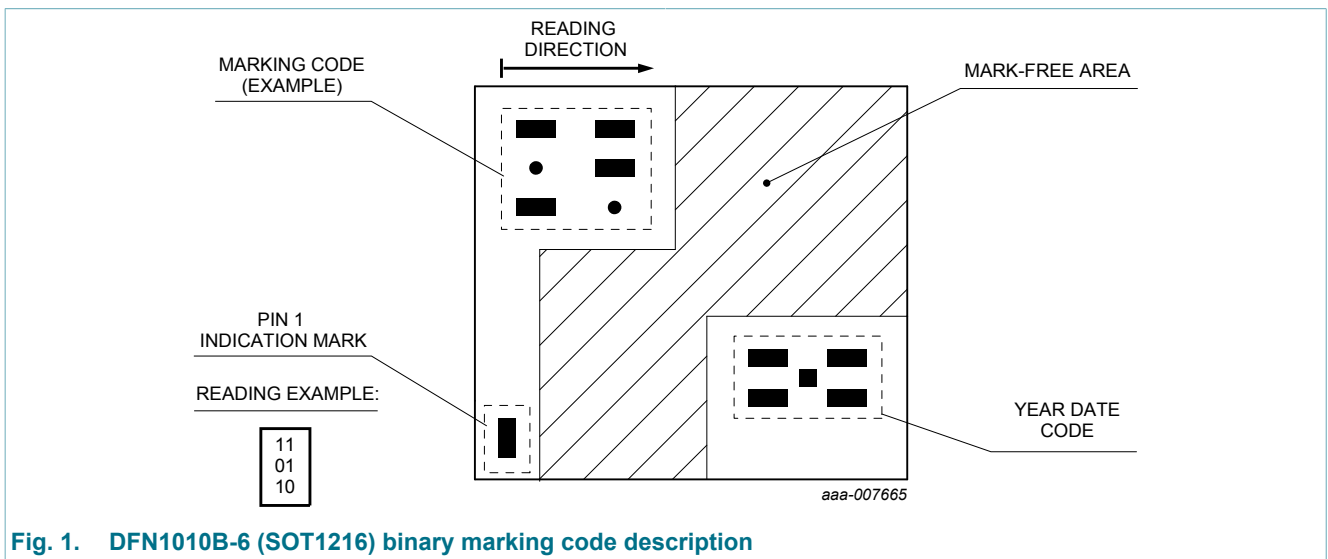
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDXB1200UPE	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

### 7. Marking

Table 4. Marking codes

Type number	Marking code
PMDXB1200UPE	11 10 00



## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	-30	V
$V_{GS}$	gate-source voltage			-8	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-410	mA
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-260	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-1.7	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	285	mW
			[1]	-	410	mW
		$T_{sp} = 25\text{ °C}$		-	4030	mW
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-410	mA
<b>Per device</b>						
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $1\text{ cm}^2$ .

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

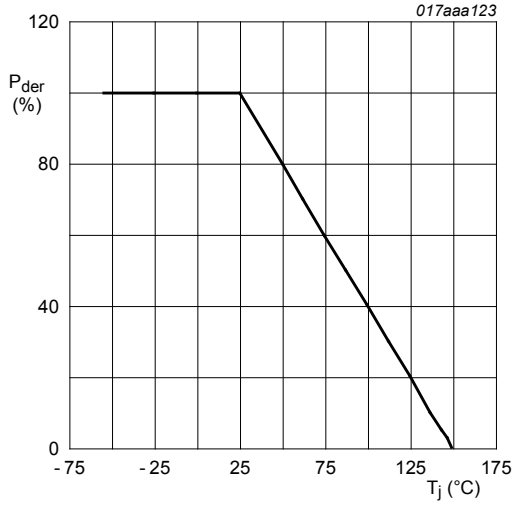


Fig. 2. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

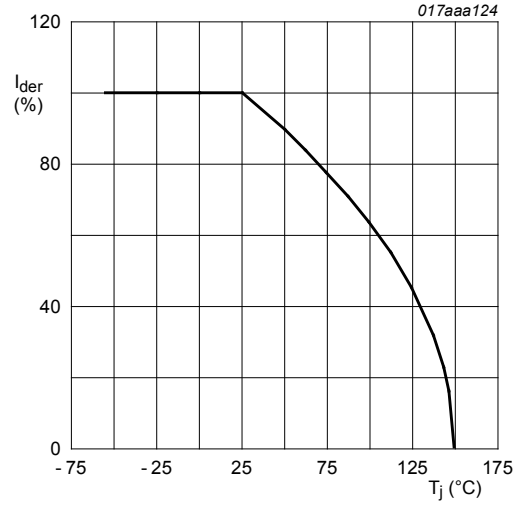


Fig. 3. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

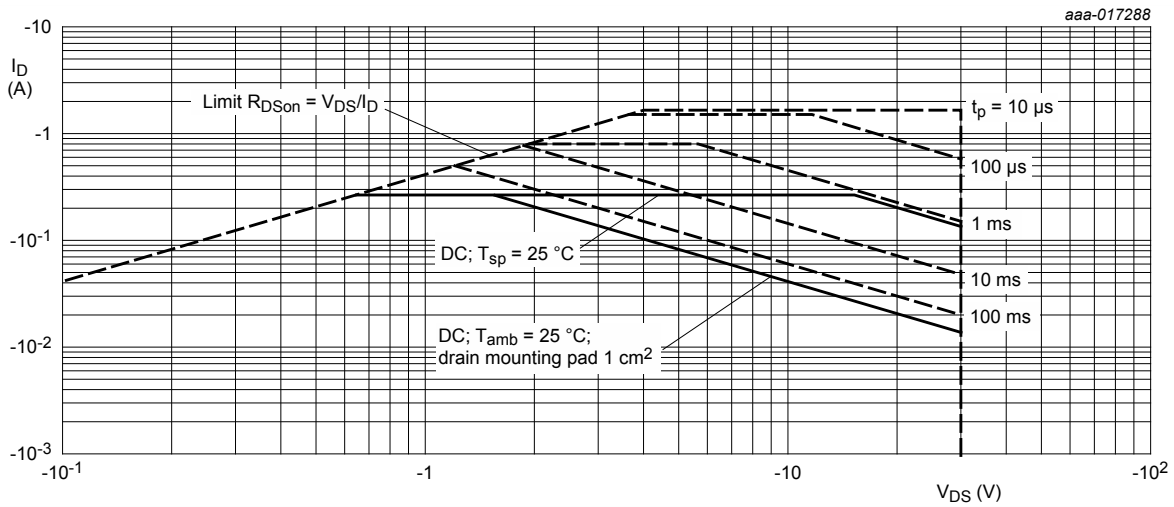


Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

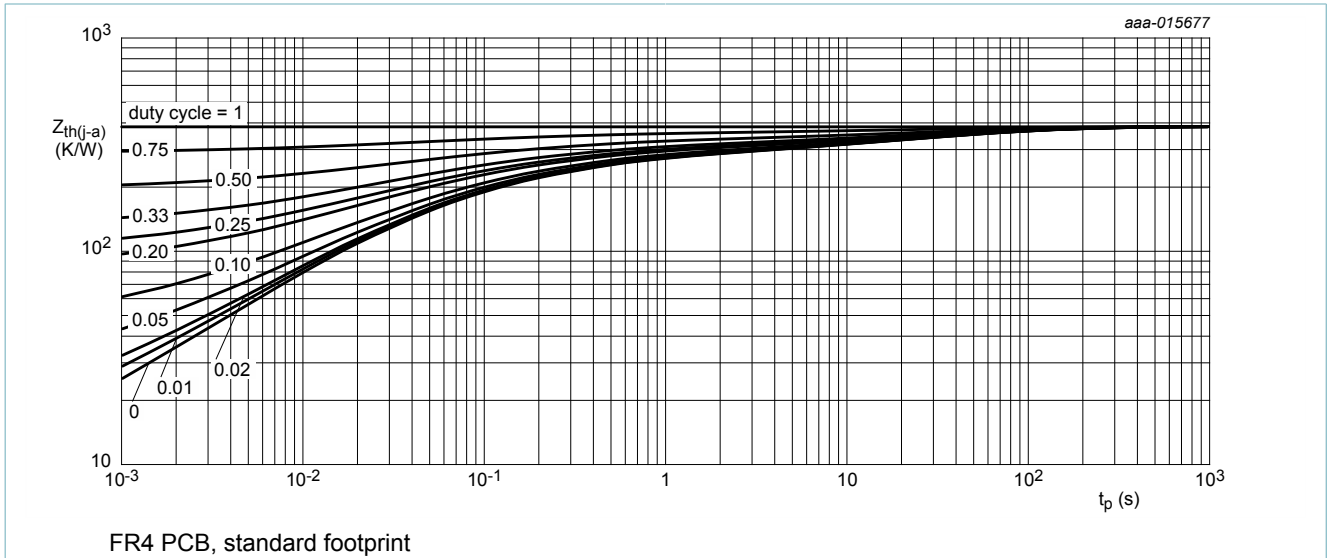
## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	380	440	K/W
			[2]	-	275	305	K/W

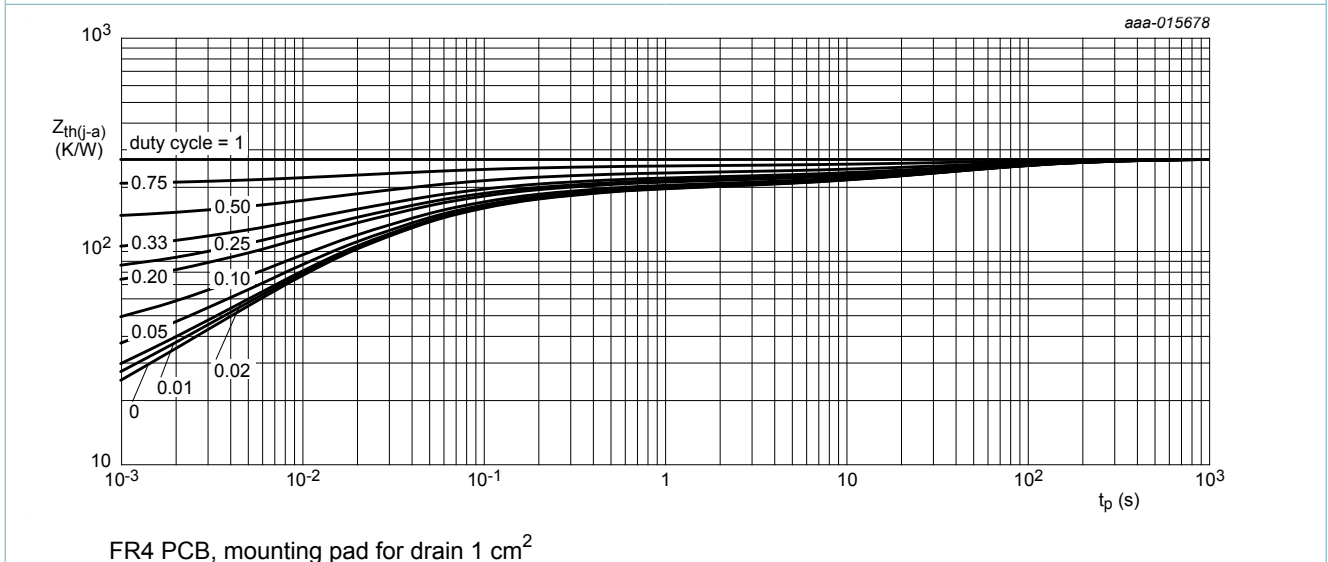
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	27	31	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



FR4 PCB, standard footprint

**Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



FR4 PCB, mounting pad for drain 1 cm<sup>2</sup>

**Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.45	-0.7	-0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	5	$\mu A$
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-5	$\mu A$
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -410 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.2	1.4	$\Omega$
		$V_{GS} = -4.5 V; I_D = -410 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	2	2.4	$\Omega$
		$V_{GS} = -2.5 V; I_D = -320 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.7	2.3	$\Omega$
		$V_{GS} = -1.8 V; I_D = -80 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2.1	3.1	$\Omega$
		$V_{GS} = -1.5 V; I_D = -10 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	3	5.1	$\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 V; I_D = -410 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	820	-	mS
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -15 V; I_D = -410 \text{ mA};$ $V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$	-	0.7	1.2	nC
$Q_{GS}$	gate-source charge		-	0.17	-	nC
$Q_{GD}$	gate-drain charge		-	0.16	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -15 V; f = 1 \text{ MHz}; V_{GS} = 0 V;$ $T_j = 25 \text{ }^\circ C$	-	43.2	-	pF
$C_{oss}$	output capacitance		-	5.9	-	pF
$C_{rss}$	reverse transfer capacitance		-	4.2	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15 V; I_D = -410 \text{ mA};$ $V_{GS} = -4.5 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	3	-	ns
$t_r$	rise time		-	4	-	ns
$t_{d(off)}$	turn-off delay time		-	14	-	ns
$t_f$	fall time		-	5	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = -410 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.95	-1.2	V

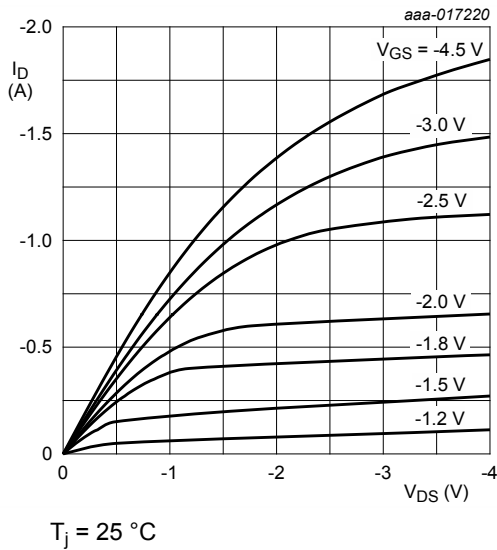


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

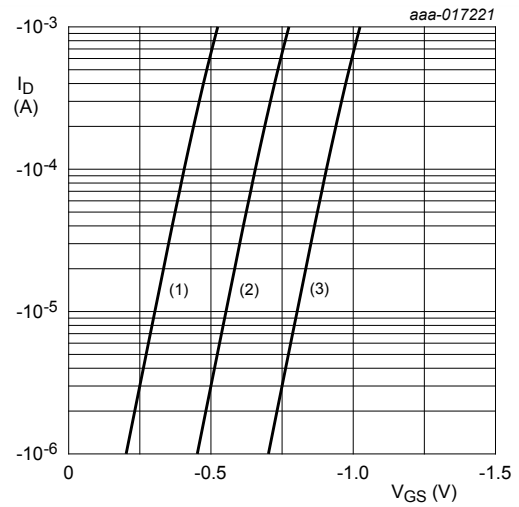


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

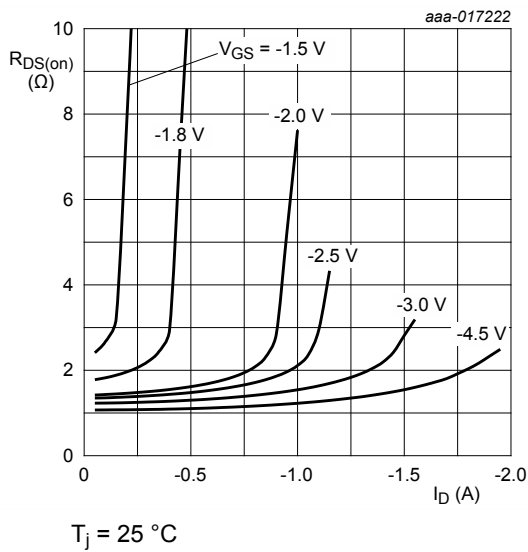


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

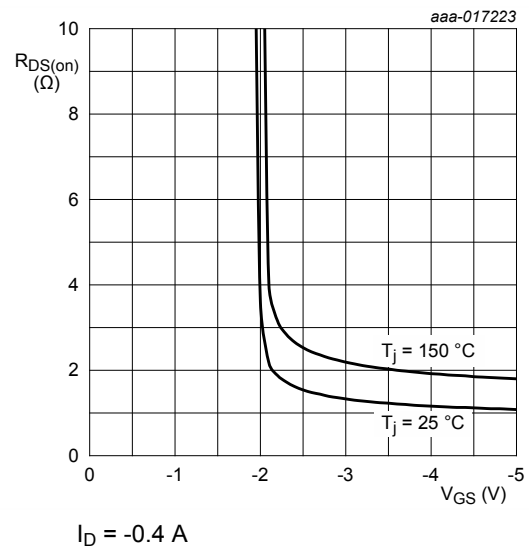
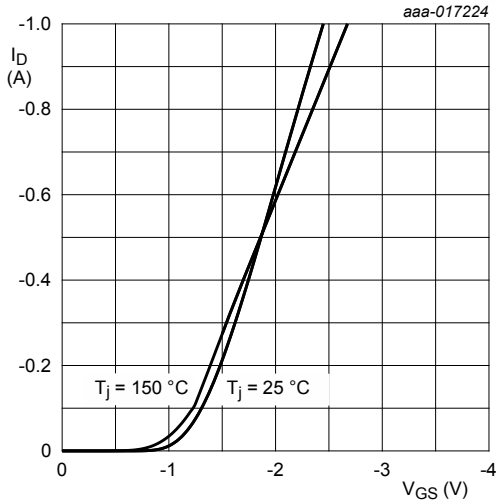


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values





$$V_{DS} > I_D \times R_{DS(on)}$$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

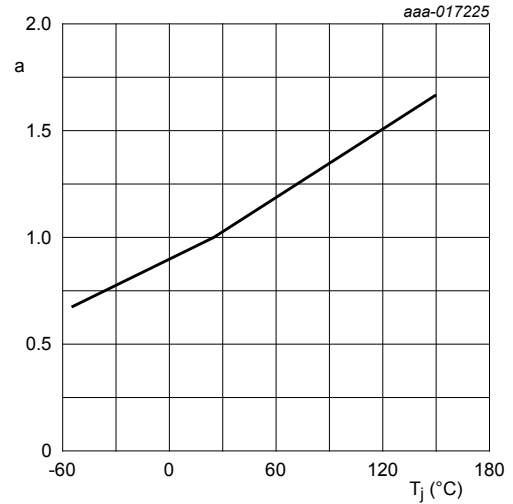
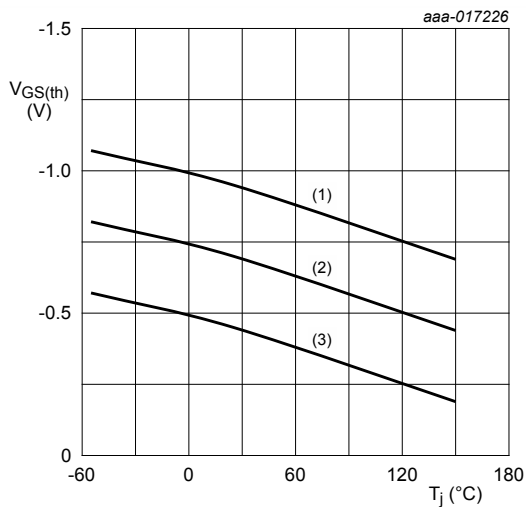


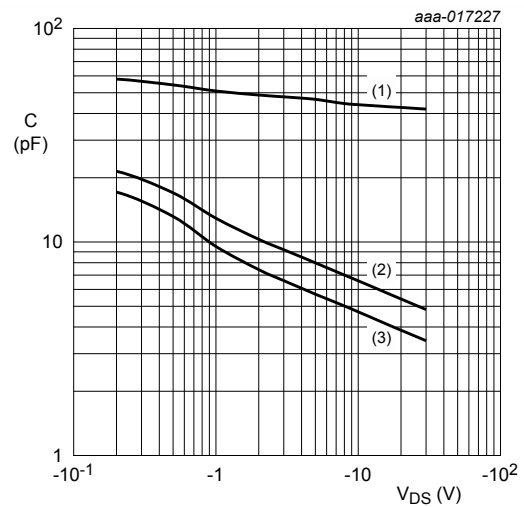
Fig. 12. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ C}}$$



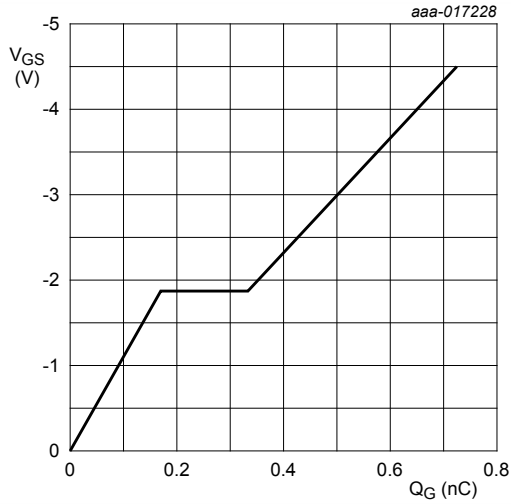
$I_D = -250 \mu A; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

Fig. 13. Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -15\text{ V}; I_D = -410\text{ mA } T_{amb} = 25\text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

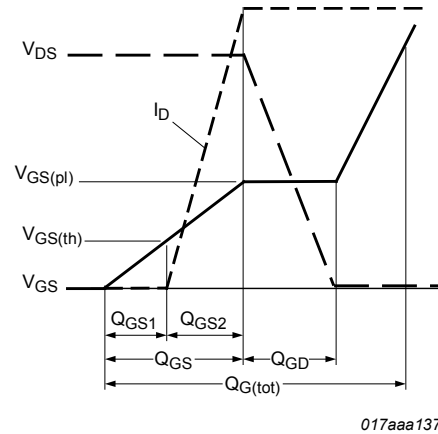
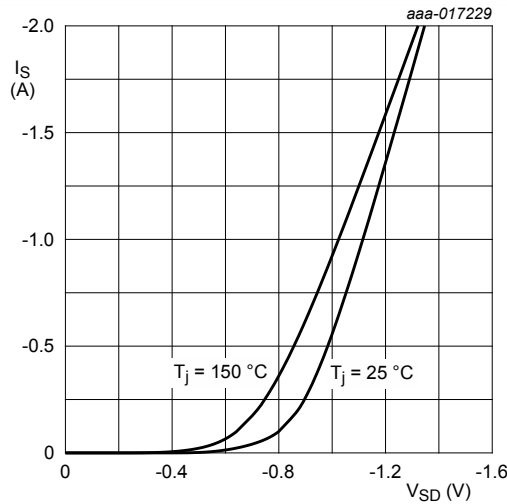


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information

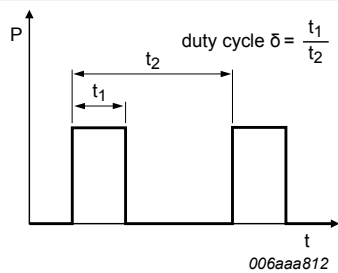


Fig. 18. Duty cycle definition

## 12. Package outline

DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads;  
6 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1216

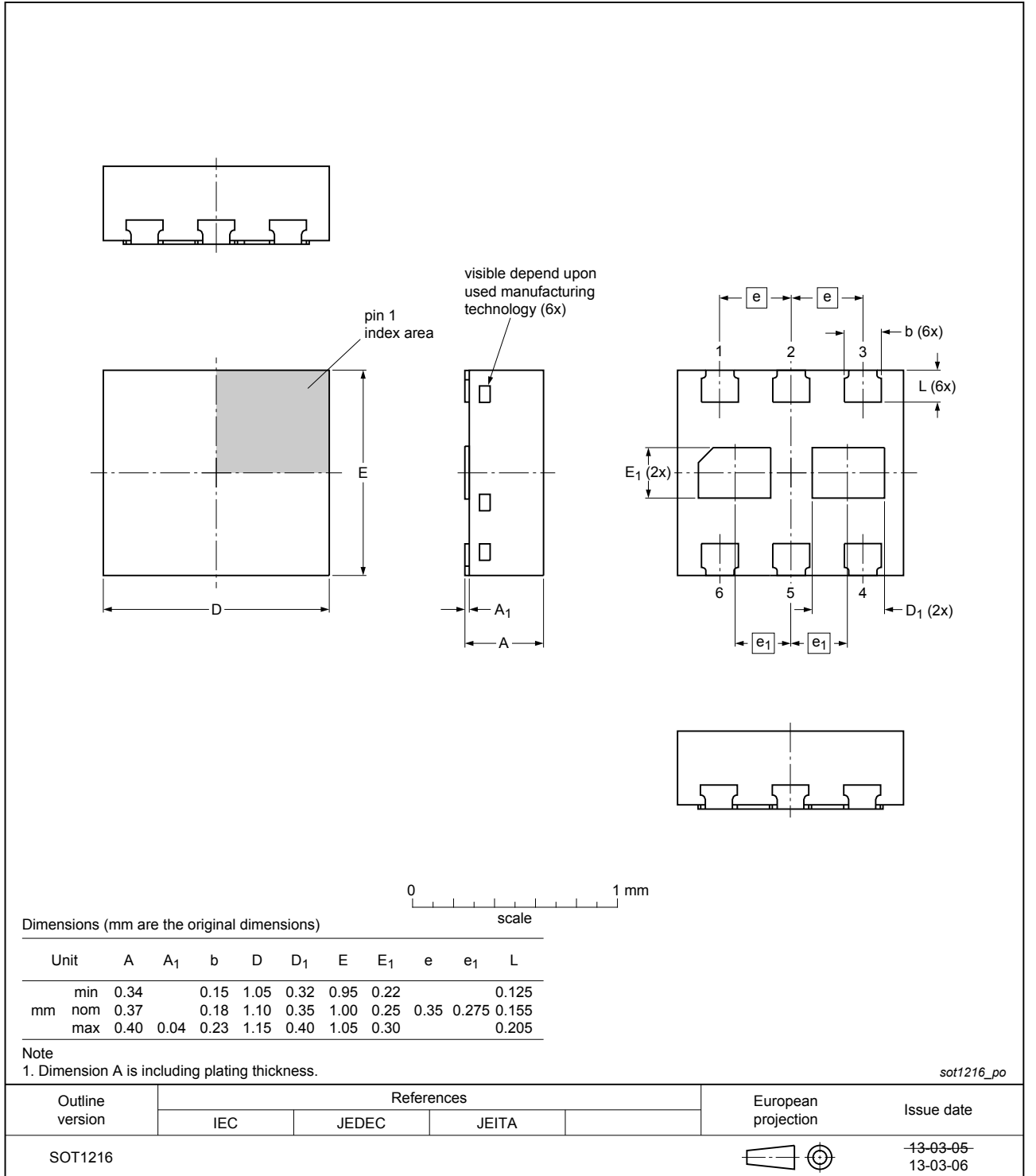


Fig. 19. Package outline DFN1010B-6 (SOT1216)

### 13. Soldering

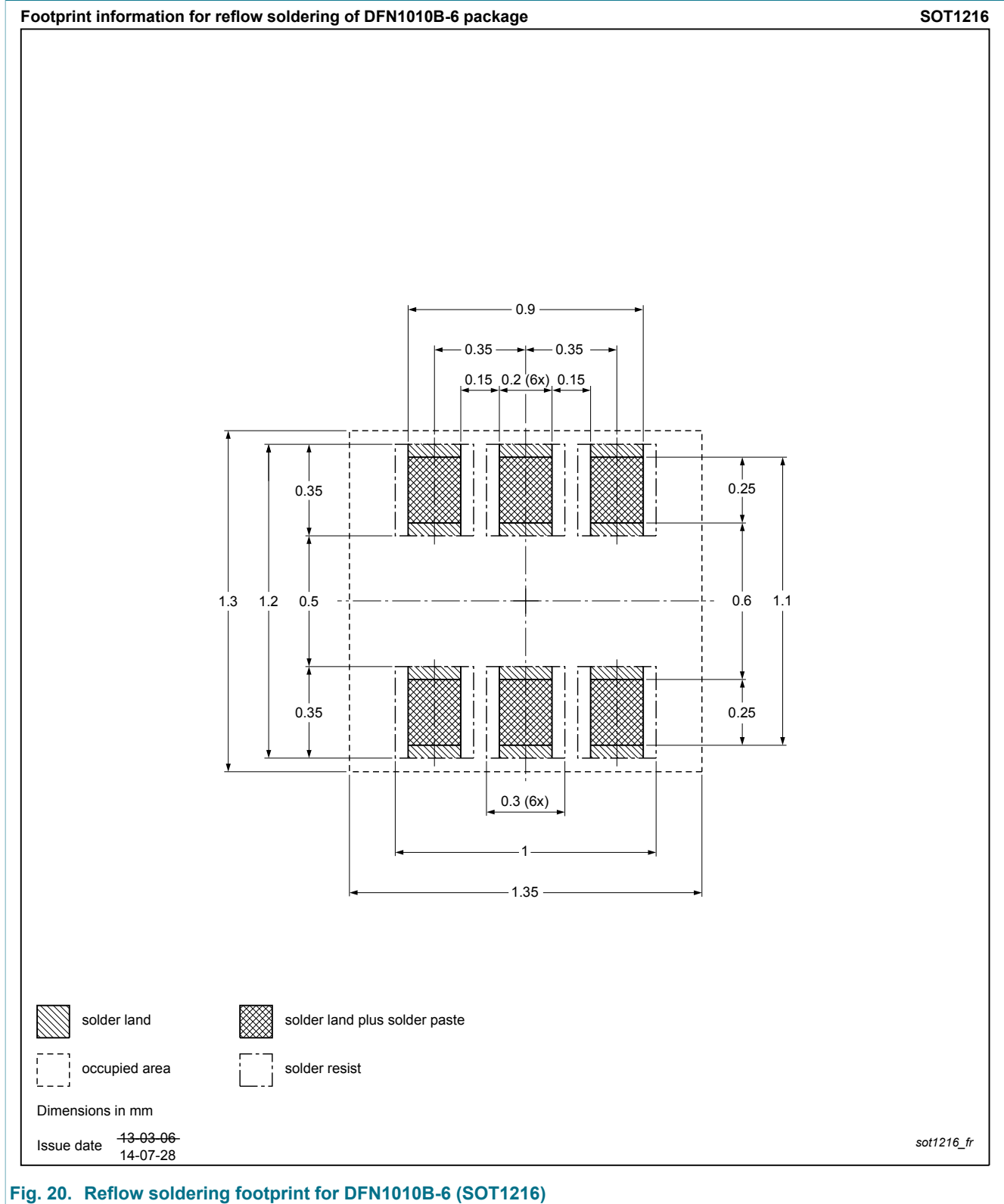


Fig. 20. Reflow soldering footprint for DFN1010B-6 (SOT1216)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDXB1200UPE v.1	20150325	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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